## REMARKS

Claims 8, 9, 12-15, 17, 19-21 and 30-32 are pending in the present application, were examined, and stand rejected. In response, no claims are amended, no claims are cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 8, 9, 12-15, 17, 19-21 and 30-32 in view of at least the following remarks. Reconsideration and withdrawal of the rejections of record are requested in view of such amendments and the following discussion.

### I. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 8-9, 12-14 and 30-32 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,477,623 ("Jeddeloh") in view of U.S. Patent No. 5,802,605 issued to Alpert et al. ("Alpert"). Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

Regarding Claim 8, Claim 8 recites the following claim features, which are neither taught nor suggested by Jeddeloh, Alpert or the references of record:

> using a conversion table to translate a first address from a graphics controller to a second address to a memory, wherein the second address has a greater number of bits than the first address. (Emphasis added.)

After carefully reviewing the entire specification of Jeddeloh, Applicants respectfully submit that Jeddeloh is silent as to an extension of a physical address beyond the 32-bit limit for conventional memory. Jeddeloh teaches:

> Graphics address relocation table (GART table) 202 is used to translate addresses from a reserve range of graphic addresses into addresses containing graphics data that are scattered throughout system memory. . . . The implementation of GART table 202 in the present invention differs from conventional implementations for GART tables in a number of ways. First, GART table 202 translates destination addresses originating from a number of different interfaces and devices coupled to switch 124. In doing so, the present

> invention tests each destination address to see if it falls within the reserved range and if so performs the address translation. This differs from conventional systems in which GART tables are used to translate only destination addresses originating from an off-chip graphics controller. (col. 6, lines 17-46.) (Emphasis added.)

Conventionally, when a graphics application required allocation of a portion of main memory for the graphics adapters' use, it issues a request to an operating system (OS) memory allocation routine, which assigns a portion of main memory, referred to as the "graphics aperture." Generally, the request for a large block of main memory results in the allocation of a series of non-contiguous pages to yield the requested block size.

Once the portion of memory is allocated, the OS returns a 32-bit linear memory start address (above the top of memory) to the graphics application and sets up a series of page table entries that will translate accesses within the linear address range to the appropriate pages of main memory. Unfortunately, when the graphics adapter attempts to access the graphics aperture, neither the graphics adapter nor the chipset between the graphics controller and main memory know where the processor's page tables are in memory. They, therefore, cannot take advantage of the processor's address translation mechanism.

In other words, when software executing on the processor, such as a graphics application, attempts to access the graphics aperture, the processor's paging mechanism automatically performs the address translation. As a result, a graphics address relocation table (GART), as described within Jeddeloh, is provided to enable the chipset to perform address translation. However, the address translation using a GART table limits the graphics devices to 32-bit physical address range.

As correctly pointed out by the Examiner, Jeddeloh does not disclose the second address having a greater number of bits than the address. As a result, the Examiner cites Alpert, which according to the Examiner, teaches a concept of using a conversion table (page table) to translate an initial address to a translated address, wherein the translated address has a greater number of bits than the initial address. (*See*, pp. 2-3 of Final Office Action mailed July 14, 2004.)

Alpert teaches a processor paging mechanism and the extension of the paging mechanism provide a 36-bit physical address range. Although Alpert teaches the expansion of addressing capability, the teachings of Alpert are strictly limited to modification of the processor's paging mechanism to expand the physical address space available for address translation. Conversely,

the teachings of Jeddeloh are strictly limited to translating destination addresses originating from off-chip graphic controllers, as well as other controllers into the physical address space.

As indicated above, the address translation techniques as taught by Alpert are distinct from the address translation of Jeddeloh since the chipset or other device coupled to the various controllers is unaware of, and does not have access to the processor's paging tables; the chipset cannot take advantage of the processor's address translation mechanism. As a result, the GART tables are provided to perform address translation of destination addresses from off-chip controllers. Hence, Applicants respectfully submit that the Examiner fails to establish a suggestion or motivation to modify or combine the reference teachings of Jeddeloh in view of Alpert. As indicated by the Federal Circuit:

> If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. In re Ratti, 270 F.2d 810, 123, U.S.P.Q. 349 (C.C.P.A. 1959).

As illustrated with reference to Table 2 of Alpert, Alpert describes the population of various processor control registers to achieve a plurality of memory management types and modes. As described with reference to col. 9, lines 35-60, Table 2 of Alpert describes population of control registers that control the processor's operational characteristics to achieve the extended address translation for a 36-bit or more physical address space. Applicants respectfully submit that the control registers referred to in Table 2 are not known or available to off-chip controllers. The processor modes described within Table 2 include:

> Mode A is the default mode. This is the mode that is compatible with all other members of the X86 family of microprocessors, including the Intel 80386 and the Intel 80486 microprocessors. Mode B represents normal addressing (less than 4 GByte) and a capability for selecting one or two page sizes. Mode C represents extended addressing (a larger physical memory) and a capability for selecting one or two page sizes. (col. 9, lines 38-45.)

Applicants respectfully submit that modification of the GART table and address translation mechanism, as taught by Alpert, would require substantial modification to the chipset to provide the various control registers and logic required to perform the extended addressing, as taught by Alpert. Furthermore, the off-chip controllers would require modification to populate the various control registers to direct the chipset to perform the extended address translation according to Table 2. Accordingly, Applicants respectfully submit that the teachings of the

combinations of Jeddeloh in view of Alpert are not sufficient to render the claims *prima facie* obvious. Id.

Accordingly, Applicants respectfully submit that the Examiner fails to establish that it would be obvious to combine the missing elements provided by Alpert with the teachings of Jeddeloh. It is also well established that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent the teaching or suggestion supporting such combination. ACS Hospital Sys., Inc. v. Montefiore Hospital, 732 F.2d. 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Moreover, one cannot find obviousness through hindsight to construct a claimed invention from elements of the prior art. In re Warner, 379 F.2d 1011, 1016, 154 U.S.P.Q. 173, 177 (C.C.P.A. 1967).

Accordingly, Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight. Therefore, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness, since the address translation provided for off-chip controllers, as taught by Jeddeloh, is completely distinct from the paging table address translation mechanism of a processor as taught by Alpert, and hence, fails to provide a suggestion or motivation to modify or combine the reference teachings.

Hence, Claim 8 is patentable over the combination of Jeddeloh in view of Alpert, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 8.

Regarding Claims 9 and 12-14, Claims 9 and 12-14 depend from Claim 8 and therefore include the patentable claim features of Claim 8. Accordingly, Claims 9 and 12-14, based on their dependency from Claim 8, are also patentable over the combination of Jeddeloh in view of Alpert, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 9 and 12-14.

Regarding Claim 30, Claim 30 recites:

> an address translator having a first interface to couple to a memory controller, a second interface to couple to a graphics controller, a third interface to couple to a bus controller, and a table of entries, each entry having a first portion and a second portion;
>
> a translation control circuit coupled to the address translator to program the entries in the address translator;
>
> wherein the address translator is to translate an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface. (Emphasis added.)

For at least the reasons described above with reference to Claim 8, the Examiner is prohibited on relying on the combination of Jeddeloh in view of Alpert, since the processor paging mechanism and address translation scheme, as taught by Alpert, is completely distinct from the address translation mechanism for destination addresses received from off-chip controllers, as taught by Jeddeloh, to require alteration of the principle of operation of Jeddeloh to achieve the modification proposed by the Examiner. Accordingly, Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight.

Therefore, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of Claim 30, since the Examiner fails to illustrate some suggestion or motivation to modify the reference or combine the reference teachings, since the reference teachings are directed to distinct mechanisms for performing address translation. Accordingly, Applicants respectfully submit that Claim 30 is patentable over the combination of Jeddeloh in view of Alpert, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 30.

Regarding Claims 31 and 32, Claims 31 and 32 depend from Claim 30 and therefore include the patentable claim features of Claim 30, as described above. Accordingly, Claims 31 and 32, based on their dependency from Claim 30, are also patentable over the combination of Jeddeloh in view of Alpert, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 31 and 32.

The Examiner has rejected Claims 15 and 17 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Alpert and further in view of U.S. Patent No. 5,574,877 issued to Dixit et al. ("Dixit"). Applicants respectfully traverse this rejection.

Regarding Claim 15, Claim 15 recites the following claim:

> control logic coupled to the translation lookaside buffer, the input register, and the output register;
>
> wherein the control logic is to compare a first portion of an initial address from a bus controller in the input register with entries in the translation lookaside buffer; and if a matching entry is found, to combine a first value associated with the matching entry with a second portion of the initial address to form a first

translated address having a greater number of bits than the initial address and hold the first translated address in the output register. (Emphasis added.)

As indicated above, the Examiner is prohibited from relying on the combination of Jeddeloh in view of Alpert, since Jeddeloh and Alpert are directed to distinct forms of address translation. In fact, modification of Jeddeloh in view of Alpert to expand the available physical address range from 32-bits to 36-bits and as much as 64-bits would alter the principle of operation of Jeddeloh. Hence, the teachings of Jeddeloh in view of Alpert are insufficient to render the claims *prima facie* obvious. Id.

Regarding the Examiner's citing of Dixit, Applicants respectfully submit that the teachings of Dixit are directed to modification of the processor's paging tables and paging mechanism for address translation. Dixit teaches a table, which has at least two page frame numbers (PFN) associated with each tag (virtual page number). Thus a match, will produce two possible physical page frame numbers. The selection between these two is controlled by a bit provided directly from the virtual address, without translation. Hence, the teachings of Dixit provide no teachings or suggestions with regards to address translation for destination addresses received from off-chip controllers.

Therefore, Applicants respectfully submit that the Examiner is similarly prohibited from relying on the combination of Jeddeloh in view of Alpert and further in view of Dixit, since the Examiner fails to illustrate some suggestion or motivation to modify the referenced teachings. Accordingly, Applicants respectfully submit that Applicants' claimed invention could only be arrived at through inappropriate hindsight.

Therefore, Claim 15 is patentable over the combination of Jeddeloh in view of Alpert and further in view of Dixit. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 15.

Regarding Claim 17, Claim 17 depends from Claim 15 and therefore includes the patentable claim features of Claim 15, as described above. Accordingly, Claim 17, based on its dependency from Claim, is also patentable over he combination of Jeddeloh in view of Alpert and further in view of Dixit, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 17.

The Examiner has rejected Claims 19-21 under 35 U.S.C. §103(a) as being unpatentable over Jeddeloh in view of Dixit. Applicants respectfully traverse this rejection.

Regarding Claim 19, Claim 19 recites the following claim feature, which is neither taught nor suggested by the combination of Jeddeloh in view of Dixit, as well as the references of record:

> control logic coupled to the translation lookaside buffer, the input register, and the output register;
>
> wherein the control logic is to compare a first portion of a first initial address from the bus controller in the input register with entries in the translation lookaside buffer; and if a first matching entry is found, to combine a first value associated with the first matching entry with a second portion of the first initial address to form a first translated address having more bits than the first initial address and hold the first translated address in the output register. (Emphasis added.)

As indicated above, the teachings of Dixit are directed to the modification of the paging tables and paging mechanism for processor address translation. Hence, the teachings of Dixit provide no teachings or suggestions with regards to address translation for destination addresses received from off-chip controllers. Likewise, Applicants respectfully submit that the assignment of two physical pages per virtual tag do not, in fact, result in a first translated address having more bits than the first initial address, but in fact provide a single physical page as selected by a bit provided directly from the virtual address without translation.

Accordingly, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of obviousness of Claim 19, since the Examiner fails to illustrate a suggestion or motivation for combining the reference teachings of Jeddeloh in view of Dixit, the Examiner also fails to illustrate that the combination of Jeddeloh in view of Dixit teaches a first translated address having more bits than the first initial address, since a bit associated with the virtual address prior to translation, selects between the two physical page frames and hence, provides a single page frame. (*See*, Abstract.)

Accordingly, Claim 19 is patentable over the combination of Jeddeloh in view of Dixit. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 19.

Regarding Claims 20 and 21, Claims 20 and 21 depend from Claim 19 and therefore include the patentable claim features of Claim 19, as described above. Accordingly, Claims 20

and 21, based on their dependency from Claim 19, are also patentable over the combination of Jeddeloh in view of Dixit. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 20 and 21.

## CONCLUSION

In view of the foregoing, it is submitted that Claims 8, 9, 12-15, 17, 19-21 and 30-32 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: September 14, 2004

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon 9/14/04
Nedy Calderon Date